CLAIMS

What is claimed is:

1. A system on a chip (SOC) integrated circuit comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions; and

at least one field programmable gate array (FPGA) cell, coupled to the plurality of peripheral functions, wherein the FPGA cell can be configured to selectively enable the plurality of peripheral functions.

2. The SOC integrated circuit of claim 1 which includes a bus coupled to the at least one FPGA cell.

3. The SOC integrated circuit of claim 2 wherein the FPGA cell can be programmed to complete connections from the bus to the peripheral functions or tie the peripheral functions to an inactive state.

4. The SOC integrated circuit of claim 3 wherein the FPGA cell programs a register coupled thereto.

5. The SOC integrated circuit on a chip of claim 1 wherein a customer can configure the FPGA cell.

6. A system on a chip (SOC) integrated circuit comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions;

a plurality of buses; and

a plurality of field programmable gate array (FPGA) cells, each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells can be configured to selectively enable a number of peripheral functions.

7. The SOC integrated circuit of claim 6 wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB)..

8. The SOC integrated circuit of claim 6 wherein the FPGA cell can be programmed to complete connections from the bus to the peripheral functions or tie the peripheral functions to an inactive state.

9. The SOC integrated circuit of claim 8 wherein the FPGA cell programs a register coupled thereto.

10. A SOC integrated circuit on a chip (SOC) integrated circuit comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions;

a plurality of buses, wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB), and

a plurality of field programmable gate array (FPGA) cells, each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells can be configured to selectively enable the portion of peripheral functions, wherein the FPGA cell can be programmed to complete connections from one of the plurality of buses to the peripheral functions or tie the peripheral functions to an inactive state, and wherein the FPGA cell is programmed through a register coupled thereto.

11. The SOC integrated circuit of claim 10 wherein the plurality of base functions comprise any combination of:

a processor, a universal interrupt controller, an SDRAM controller, an on-chip controller (OCM), an SRAM, a PLB arbiter, an OPB arbiter, an OPB bridge, and a UART.

12. The SOC integrated circuit of claim 11 wherein the plurality of peripheral functions comprise any combination of:

an external bus controller (EBC), an SDRAM controller, a proprietary function, a peripheral controller, an I^2C interface, and a second UART, a DMA controller, a media access layer (MAL) function, and a plurality of media access controllers (MACs).